A TRUE OFF-SET SELF-ALIGNED PROCESS FOR HIGH EFFICIENCY Ku-BAND POWER FETS (1)

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ABSTRACT

A new off-set self-aligned process has been used to fabricate a 2 x 3000 μm gate width internally matched power FET which at 14 GHz has produced 34.4 dBm output power, 6 dB gain and 32 % added efficiency at the -1 dB gain compression point with a power combining efficiency of ≈ 96 %. The high combining efficiency is attributed to the close parameter match of the self-aligned power FETs.

INTRODUCTION

Today's commercially available power FETs operating at Ku-band employ a combination of epitaxialy grown or ion implanted active layers which require single or multiple recess structures ranging in depth from 1600 Å to 4000 Å (1-8). These structures demand strict controls on the active layer fabrication, lithography and gate recess formation in order to obtain repeatable DC and RF parameters. Several self-aligned processes have been recently developed for digital and low noise applications (9,10,11). Because the ohmic (or n^+) contact regions are adjacent to the gate, high drain bias - such as required for power operation - is not possible. A process with source-gate self-alignment and advanced substrate technology has recently demonstrated excellent large signal performance (12).

This work describes and demonstrates a process whereby the source, gate, and drain openings are defined simultaneously. The source-gate self-alignment permits a relatively shallow gate recess (0-600 Å) which preserves the uniformity of the active layer. The self-aligned gate-drain spacing results in a large and uniform gate-drain breakdown voltage which is specially important for power applications.

PROCESS DESCRIPTION

The principal fabrication steps of the new process are depicted in Figure 1.

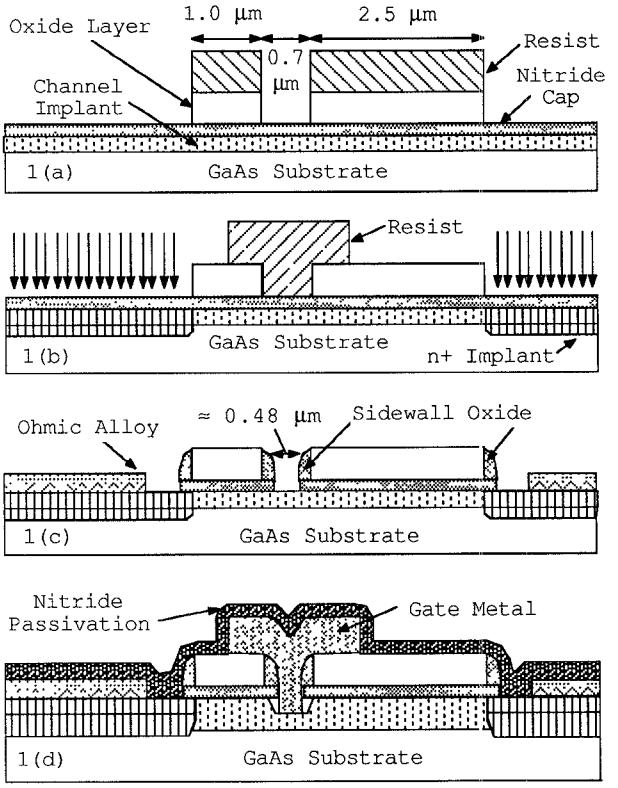

Figure 1: Cross sectional view of the self-aligned process: 1(a): after channel implant, nitride cap, anneal, first oxide deposition and self-aligned patterning steps. 1(b): after n^+ implant. 1(c): after second oxide deposition (sidewall), oxide and nitride etch, and ohmic alloy. 1(d): after gate definition, and final passivation.

After a selective Si implant, a Si_3N_4 cap is deposited to prevent GaAs decomposition during furnace annealing. The peak carrier concentration is $\approx 2x10^{17}$ Si atoms/cm^3. The channel thickness is $\approx$ 2500 Å thick. An SiO_2 layer is sputter deposited and patterned with the self-aligned source, gate and drain openings. The digitized source to gate and gate to drain spacings are 1 and 2.5 µm respectively. The gate opening is 0.7 µm. Refer to Figure 1(a). The SiO_2 is selectively removed from the openings using CHF_3 RIE. The gate area is masked with photoresist to protect it from the high energy, high dose n^+ implant of the source and the drain contact regions as in Figure 1(b). After the n^+ region is annealed, a second layer of SiO_2 is deposited on the self-aligned source, gate and drain pattern. RIE is again employed to remove the second SiO_2 layer and the nitride cap. Because the vertical reactive ion etch rate is greater than the lateral etch rate, the gate opening can be controlled by increasing or decreasing the thickness of the second oxide. Thus, sub-half-micron gate openings are made possible without having to resort to sub-half-micron lithography. A cross sectional view of the sidewall oxide is shown by Figure 1(c). The uniformity of the gate length across a wafer is depicted by Figure 2; the second SiO_2 thickness is $\approx$ 3000 Å in this case.

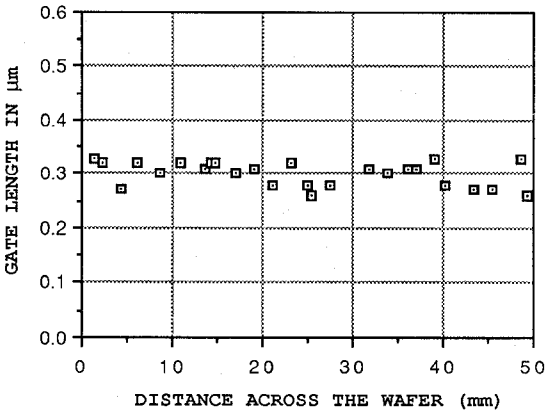

Figure 2: Typical gate length variation across a 50 mm diameter wafer.

After ohmic contacts are formed using standard alloy techniques, the gate opening is patterned and a shallow gate recess ($\leq$ 600 Å) is defined in the channel area. The recess depth, and the size of the gate metallization are controlled to optimize Rds, Cgd and alignment requirements. Ti-Pt-Au is used as the gate metallization. A Si_3N_4 layer is deposited using plasma enhanced CVD as a final passivation dielectric, as shown in Figure 1(d). The sources are interconnected using an airbridge plating process. After thinning the wafer to $\approx$ 30 µm to reduce the thermal resistance, via holes are patterned and etched through to the source contacts. The

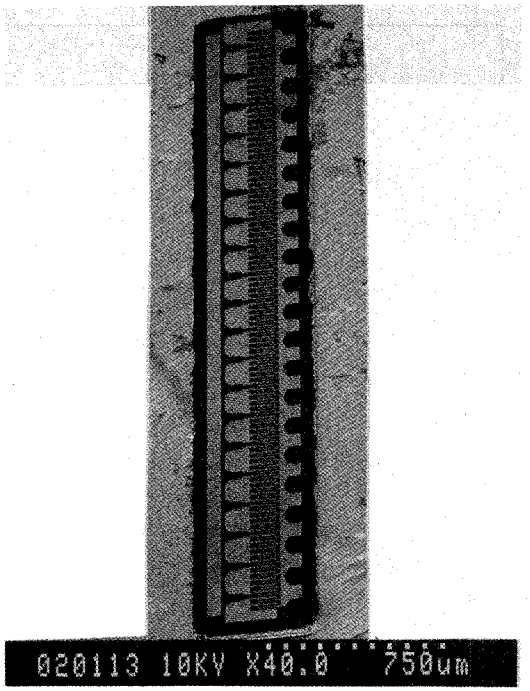

Figure 3: 16 mm gate periphery self-aligned power MESFET. The chip size is $\approx$ 500 µm x 3400 µm.

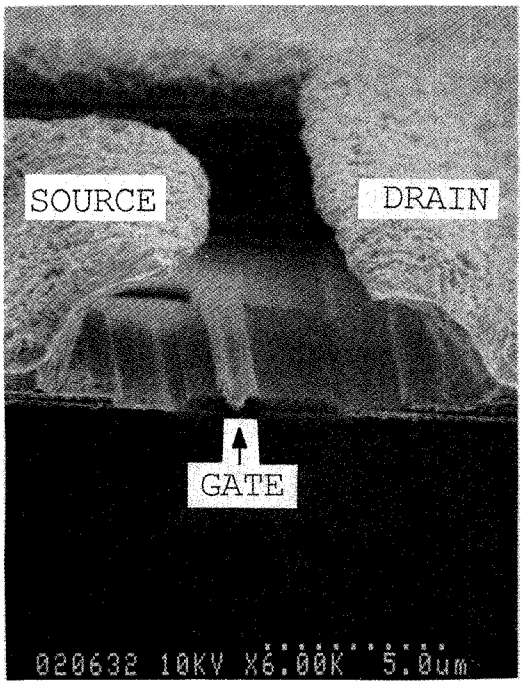

Figure 4: Cross section of finished chip showing the self-aligned structure (center).

backside is plated with Au and the wafer is then separated into chips using a dry chemical process. This technique reduces damage to the chips produced by standard scribe and separation techniques.

FETs with up to 16 millimeter gate widths have been fabricated using this process (see Figure 3.) The cross section of a finished device is shown by Figure 4. The second oxide layer deposition has been adjusted to give a final gate length ≈ 0.48 µm.

MICROWAVE RESULTS

Figure 5 shows the small signal model for a typical 750 µm monitor FET under power bias measured from 1 to 18 GHz using microwave probes.

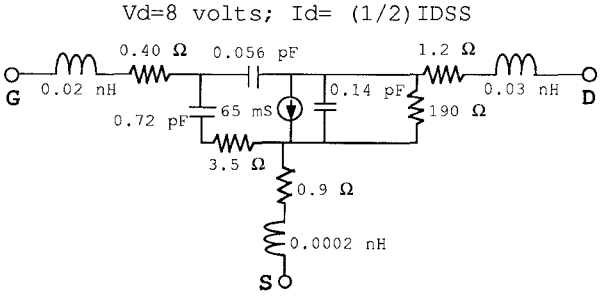

Figure 5: Small signal model for 750 µm monitor FET; from microwave probe measurement from 1 to 18 GHz.

An internally matched power FET fabricated using two 3000 µm gate width FETs has been tested at 14 GHz. The bias point was 50 % IDSS (800 mA) and Vd = 8 volts. The power and efficiency curves for this device are depicted by Figure 6: at the -1 dB gain compression point, the device produces 34.4 dBm power and 6 dB gain with η_{add} ≈ 32 %. Psat is ≈ 34.8 dBm or 503 mW/mm.

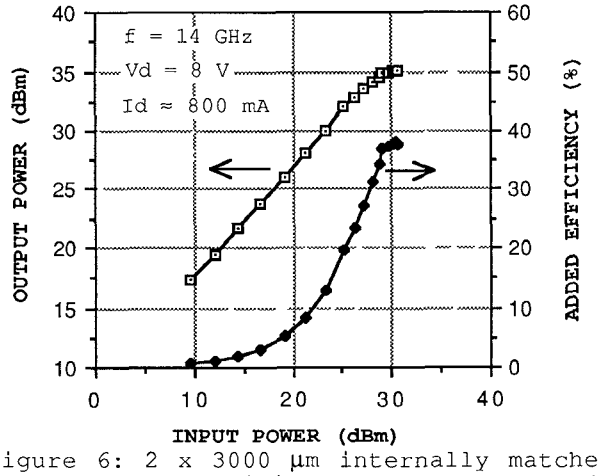

Figure 6: 2 x 3000 µm internally matched FET power and efficiency performance at 14 GHz. Linear gain is ≈ 7 dB.

Figure 7 shows a similarly biased 750 µm monitor FET. In this case, Psat ≈ 25.92 dBm, or ≈ 521 mW/mm. These results suggest that the power combining efficiency is better than 96 % for the IMFET. This achievement is attributed to the close parameter match resulting from using the new self-aligned process.

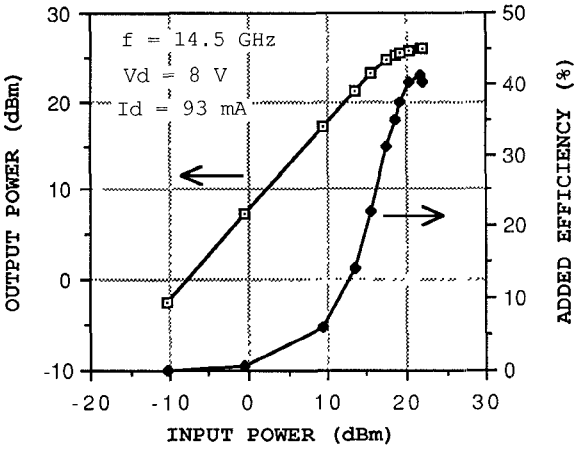

Figure 7: 750 µm monitor FET power and efficiency performance at 14.5 GHz. Linear gain is ≈ 7.8 dB.

The 750 µm monitor FET has also been evaluated at other frequencies and bias conditions. The results are summarized in TABLE(I).

FREQ. (GHz)	P-1 dB (dBm)	G-1 dB (dB)	EFFICIENCY (%)	Vd (V)	Id
8	25.7	10.5	35	8	0.5IDSS
9.5	25.1	9	32	8	0.5IDSS
9.5	25.3	6.1	40	8	0.2IDSS
14.5	25.3	6.8	35	8	0.5IDSS
18	24.6	5.4	25	8	0.5IDSS
18	25.1	3	31	8	0.2IDSS

TABLE (I): 750 µm Monitor FET with IDSS ≈ 200 mA.

RELIABILITY

The drain to source burn-out voltage characteristics of a typical power FET were measured at room temperature using a Tektronix 370 programmable curve tracer. The pulse width was 80 µs and the duty cycle was 100 Hz. Catastrophic failures occurred at Vd ≈ 15, 27 and 30 volts for 100% IDSS, 50% IDSS and pinch-off (defined at Vd = 2 volts and 1.5% IDSS) respectively.

After 3000 hours of High Temperature Storage (HTS) at 295 °C in air, the average drift of the critical parameters for a

sample of five FETs was as follows: $\Delta IDSS \approx -15\ \%$, $\Delta Gm \approx -8\ \%$ and $\Delta Vpo \approx -9\ \%$.

These results are attributed to the triple passivation of the active area. First, the channel is covered with a layer of nitride which is used as the capping material during the channel anneal. Second, a layer of oxide is deposited on the cap and used to pattern the self-aligned source gate and drain openings, and finally, a film of silicon nitride is deposited by plasma enhanced Chemical Vapor Deposition to assure hermeticity.

CONCLUSIONS

A new off-set self-aligned process for the fabrication of power FETs has been demonstrated (efforts are now under way to improve the active layer for 18 GHz operation, test discrete devices with 16 mm gate widths, and implement power MMICs.) The new process has been used, but is not limited to, the production of analog microwave devices.

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